AF/2811 ofw



Docket No.: 57454-948 PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

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|---|---|---|
| In re Application of | : | Customer Number: 20277 |
| Tomohide TERASHIMA | : | Confirmation Number: 2683 |
| Application No.: 10/647,288 | : | Tech Center Art Unit: 2811 |
| Filed: August 26, 2003 | : | Examiner: Pham, Long |
| For: SEMICONDUCTOR DEVICE | : | |

**TRANSMITTAL OF APPEAL BRIEF**

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

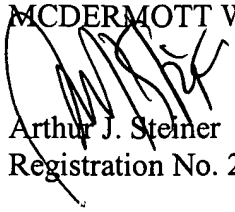
Sir:

Submitted herewith is Appellant's Appeal Brief in support of the Notice of Appeal filed October 4, 2004. Please charge the Appeal Brief fee of $340.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP



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**Date: October 7, 2004**

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## APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed October 4, 2004.

## I. REAL PARTY IN INTEREST

The real party in interest is Mitsubishi Denki Kabushiki Kaisha.

## II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any related Appeal or Interference.

## III. STATUS OF CLAIMS

Claims 1 through 6 are pending in this Application. Claims 3, 5, and 6 have been allowed. Claims 1, 2 and 4 have been finally rejected. Appellant hereby appeals from the final rejection of claims 1, 2 and 4.

## IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the July 7, 2004 Office Action in which claims 1, 2 and 4 were finally rejected. A Request for Reconsideration was submitted on September 1, 2004. The Examiner issued an Advisory Action dated September 16, 2004 maintaining the final rejection of claims 1, 2 and 4.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1, the only independent claim, is directed to a semiconductor device comprising, *inter alia*, first and second field-effect transistors functioning as high side switches of a latch circuit and sharing a common source region (page 1 of the written description of the specification, line 25 through page 2, line 3). This type of structure enables reduction of the area of the element formation region where the high side switch of the latch circuit is formed, thereby facilitating further miniaturization of the semiconductor device (first paragraph on page 2 of the written description).

## VI. GROUNDS OF REJECTION TO BE REVIEWED BY APPEAL

Claims 1, 2 and 4 were rejected under 35 U.S.C. § 103 for obviousness predicated upon Otake in view of Daniel et al.

## VII. ARGUMENT

For the convenience of the Honorable Board, the patentability of claims 1, 2 and 4 stands or falls together with independent claim 1.

As previously mentioned, the semiconductor device defined in independent claim 1 comprises, *inter alia*, first and second field-effect transistors functioning as high side switches of a latch circuit and sharing a common **source** region. The Examiner admits, as he must, that Otake's semiconductor device does **not** comprise first and second field-effect transistors which share a common **source** region. Instead, in Otake's device, the transistors share a common **drain**, manifestly because Otake purposely structure the device so that the transistors share a common **drain.** But that is not good enough for the Examiner. The Examiner would deviate from and proceed **against** the expressed teachings of Otake. How does the Examiner do that?

The Examiner has served up the conclusion that one having ordinary skill in the art would have been motivated to **proceed against**, repeat **proceed against**, the teachings of Otake by **restructuring** Otake's device to form first and second field-effect transistors which share a common source region -- not a common drain region as expressly disclosed and purposely structured by Otake. But in order to establish the requisite motivation, the Examiner is required to make clear and particular factual findings as to a specific understanding or specific technological principle and, based upon such facts, explain **why** one having ordinary skill in the art would been realistically impelled to modify the **particular** semiconductor device disclosed by Otake to arrive at the claimed invention. *Teleflex Inc. v. Ficosa North America Corp., 299 F.3d 1313, 63 USPQ2d 1374, Ecolochem Inc. v. Southern California Edison, Co., 227 F.3d 1361, 56 USPQ2d 1065 (Fed. Cir. 2000); In re Kotzab, 217 F.3d 1365, 55 USPQ 1313 (Fed. Cir. 2000); In re Dembiczak, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999).*

But the Examiner did not provide any such factual basis to support the asserted motivation. The nutritionless reason presented by the Examiner is that his proposed restructuring of Otake's device such that the field-effect transistors share a common source region, rather than sharing a common drain as desired by Otake, would " . . . achieve reduction in circuit size and current consumption" (page 3 of the July 7, 2004 final Office Action, lines 4 and 5). Appellant, however, questions the **factual basis** for the Examiner's conclusion that having the field-effect transistors share a common source rather than a common drain would "achieve reduction in circuit size and current consumption." In other words, what is the factual basis upon which to conclude that somehow exchanging a common drain region, which is what Otake wants, for a common source region, would suddenly "achieve reduction in circuit size and current consumption"?

The **only factual basis** offered by the Examiner is claim 18 and paragraph [0007] of Daniel et al., the allegedly teaching reference said to disclose sharing a common source region. However, it is not apparent wherein either claim 18 of Daniel et al. or paragraph [0007] thereof link the sharing of a common source region to any "reduction in circuit size and current consumption", let alone factually establish that by **exchanging** a common drain, which is what Otake wants, for a common source, would result in any conceivably "reduction in circuit size and current consumption." Accordingly, the Examiner clearly failed to provide the requisite factual basis to support the asserted motivation.

In this respect Appellant would rely upon *Teleflex Inc. v. Ficosa North America Corp., 63 USPQ2d at 1387,* wherein the Court held:

> The showing of a motivation to combine must be clear and particular, and it must be supported by actual evidence.

Clearly, the Examiner did not provide the requisite factual basis to support the asserted motivation.

**Otake want the first and second field-effect transistors to share a common drain.**

The reason Otake's device contains first and second field-effect transistors sharing a common **drain** is because sharing a common drain is essential for the disclosed Double Diffused Metal Oxide Semiconductor (DMOS) device disclosed by Otake et al. Significantly, the Examiner does **not** dispute, or offer any technological arguments inconsistent with, Appellant's argument submitted in the September 1, 2004 Request for Reconsideration that it is essential for the DMOS device disclosed by Otake for the transistors to share a common **drain**. Appellant stresses that one having ordinary skill in the art would **not** have been realistically led to modify Otake's DMOS device so that the first and second field-effect transistors would share a common source region, because such a modification is completely **antagonistic** to Otake's objective. **Again, the Examiner does not deny this.**

The reason why one having ordinary skill in the art would not have been motivated to modify Otake's DMOS device so that the first and second field-effect transistors would share a common source region, and why such a modification is inconsistent with Otake's objective, is if the drain regions of Otake's DMOS device are divided, the resulting device would not be a DMOS device which is what Otake wants. The Examiner cannot duck this issue by asserting, as he did in the first enumerated section under the caption "Response to Arguments A" on page 2 of the September 16, 2004 advisory action.

> . . . the rejection does not require the drains to be separated or divided.

**But what does the rejection require?**

Appellant submits that the Examiner's rejection is not articulated with clarity. Is the Examiner suggesting that one having ordinary skill in the art would have restructured Otake's device so that the first and second field-effect transistors share a common source and **not** a common drain? If this is the case, then the drain regions of Otake's DMOS device must be **separated** and, if they are separated, the

resulting device is **not** a DMOS device which is what Otake wants. Alternatively, **if** the Examiner is suggesting that one having ordinary skill in the art would have been motivated to modify Otake's DMOS device such that the first and second field-effect transistors would share **both** a common source and a common drain, then the Examiner conspicuously avoided responding to Appellant's challenge to provide **objective evidence** to establish that such a resulting device is even **feasible or workable**. No such evidence has been forthcoming.

Appellant, therefore, submits that one having ordinary skill in the art would **not** have been realistically motivated to modify Otake's DMOS device such that the first and second field-effect transistors would share a common **source** rather than a common **drain**, because any such modification is completely **inconsistent** with the expressed disclosure of Otake and would undo Otake's DMOS device. *In re Fritch, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992); In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); In re Schulpen, 390 F.2d 1009; 157 USPQ 52 (CCPA 1968).* In an abundance of caution, Appellant also submits that one having ordinary skill in the art would not have been realistically motivated to modify Otake's DMOS device so that the first and second field-effect transistors share **both** a common source and both a common drain, absent any hard objective evidence to establish that one having ordinary skill in the art would have harbored any **realistic expectation of successfully obtaining a workable device**. *Valander v.Gardner, 34 F.3d 1359, 68 USPQ2D 1769 (Fed. Cir. 2003); In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

**Indicium of Nonobviousness**

Appellant submits that Otake **clearly teaches away** from the claimed invention by requiring the transistors to share a common drain, as they must, for Otake to achieve his objective of providing a DMOS structure. This clear **teaching away** from the claimed invention constitutes a potent indicium

of **nonobviousness**. *In re Bell, 991 F.2d 781, 26 USPQ2d 1529 (Fed. Cir. 1993); Specialty Composites v. Cabot Corp., 845 F.2d 981, 6 USPQ2d 1601 (Fed. Cir. 1988); In re Hedges, 783 F.2d 1038, 228 USPQ 685 (Fed. Cir. 1986); W. L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); In re Marshall, 578 F.2d 301, 198 USPQ 344 (CCPA 1978).*

## VIII. CONCLUSION

Based upon the foregoing Appellant submits that the Examiner failed to establish a *prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. § 103 for lack of the requisite factual basis and want the requisite realistic motivation. Moreover, upon giving due consideration to the clear **teaching away** from the claimed invention by the primary reference to Otake, the conclusion appears inescapable that one having ordinary skill in the art would **not** have found a claimed invention **as a whole** obviousness within the meaning of 35 U.S.C. 103.

Appellant, therefore, solicits the Honorable Board of Patent Appeals and Interferences to reverse the Examiner's rejection of claims 1, 2 and 4 under 35 U.S.C. § 103 for obviousness predicated upon Otake in view of Daniel et al.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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**Date: October 7, 2004**

## CLAIMS APPENDIX

1. A semiconductor device comprising:

an element isolation part surrounding one element formation region when viewed in the direction perpendicular to a main surface of a semiconductor substrate,1and electrically isolating the one element formation region from another element formation regions; and

a plurality of elements provided in said element formation region, wherein

said plurality of elements includes a first field-effect transistor and a second field-effect transistor functioning as high side switches of a latch circuit,

said semiconductor device is utilized in the state where a lower side of one of said first field-effect transistor and said second field-effect transistor is completely depleted, and

said first field-effect transistor and said second field-effect transistor share a source region.

2. The semiconductor device according to claim 1, wherein said first field-effect transistor and said second field-effect transistor are P-channel field-effect transistors, respectively.

3. A semiconductor device comprising:

an element isolation part surrounding one element formation region when viewed in the direction perpendicular to a main surface of a semiconductor substrate, and electrically isolating the one element formation region from another element formation regions; and

a plurality of elements provided in said element formation region, wherein

said plurality of elements includes a first field-effect transistor and a second field-effect transistor functioning as high side switches of a latch circuit,

said semiconductor device is utilized in the state where a lower side of one of said first field-effect transistor and said second field-effect transistor is completely depleted,

said first field-effect transistor and said second field-effect transistor share a source region or a drain region.

said first field-effect transistor is a P-channel field-effect transistor, and

said second field-effect transistor is a P-channel insulated gate bipolar transistor.

4. The semiconductor device according to claim 1, wherein

said first field-effect transistor is a P-channel field-effect transistor, and

said second field-effect transistor is an N-channel field-effect transistor.

5. A semiconductor device comprising:

an element isolation part surrounding one element formation region when viewed in the direction perpendicular to a main surface of a semiconductor substrate, of a first conductivity type and electrically isolating the one element formation region from another element formation regions; and

a plurality of elements provided in said element formation region, wherein:

said plurality of elements includes a first field-effect transistor and a second field-effect transistor functioning as high side switches of a latch circuit;

said semiconductor device is utilized in the state where a lower side of one of said first field-effect transistor and said second field-effect transistor is completely depleted;

said first field-effect transistor and said second field-effect transistor share a source region or a drain region;

an impurity diffusion layer of a second conductive type, formed on the semiconductor substrate of the first conductive type so as to cover the semiconductor substrate of the first conductive type, on which said first field-effect transistor and said second field-effect transistor are provided;

an impurity diffusion region of the first conductive type formed inside the impurity diffusion layer of the second conductive type and connected to a source electrode or a drain electrode of one of said first field effect transistor and said second field-effect transistor; and

an impurity diffusion region of the second conductive type, having an impurity concentration higher than that of said impurity diffusion layer of the second conductive type, located between the impurity diffusion region of the first conductive type and said semiconductor substrate of the first conductive type.

6. A semiconductor device comprising: a first field-effect transistor having a channel region of a first conductive type and a gate electrode; and a second field-effect transistor having a channel region of a second conductive type which is a conductive type opposite to said first conductive type and a drain electrode,

the gate electrode of said first field-effect transistor and the drain electrode of said second field-effect transistor being integrally formed of the same conductive layer and extending in sequence in a predetermined direction in a linear manner, and

the source electrode of said first field-effect transistor and the source electrode of said second field-effect transistor being integrally formed of the same conductive layer and extending in sequence in a predetermined direction in a linear manner, wherein

the difference in potential between the source electrode of said first field-effect transistor and the drain electrode of said second field-effect transistor is approximately the same as the difference in potential between the gate electrode and the source electrode of said first field-effect transistor, and

the punch through voltage between an impurity diffusion region of the second conductive type beneath the drain electrode of said second field effect transistor and the impurity diffusion region of the second conductive type beneath the gate electrode of said first field-effect transistor is greater than the

difference in potential between the source electrode of said first field-effect transistor and the drain electrode of said second field-effect transistor.